IOWA STATE UNIVERSITY
College of Engineering

mm-Wave Image Radar

Senior Design December 2023 - Team 20
Client/Advisor: Dr. Mohammad Tayeb Al Qaseer

Team Members/Roles:
Matt Caron - PCB design
Nathan Ayers - User Interface
Rodrigo Romero - SPI Implementation (FPGA)
Michael Levin - DSP (FPGA)

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Problem Statement

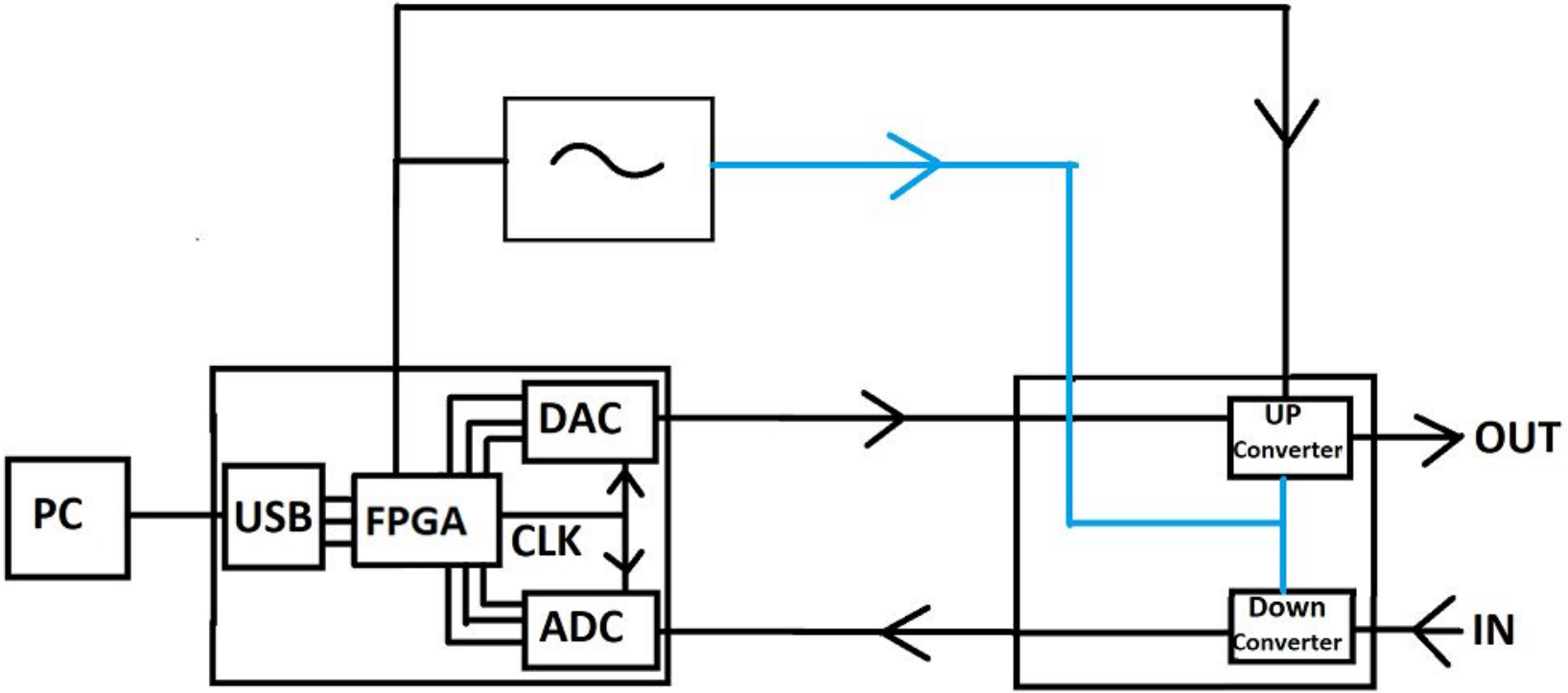
Who? Our client, Dr. Tayeb and the CNDE conduct research into evaluating a system or structure without affecting its future usability and functionality.

What? The CNDE needs a new mm-Wave radar to be built for student research experiments.

Why? Millimeter-Wave technology has been used to penetrate dielectric materials and has a high sensitivity to small material flaws. Research benefits safety and can help companies increase sustainability.

When? Students are already experimenting with samples that have errors designed to test the imaging. The applications will continue to grow and the technology will impact everyone.

Conceptual Sketch



Functional Requirements

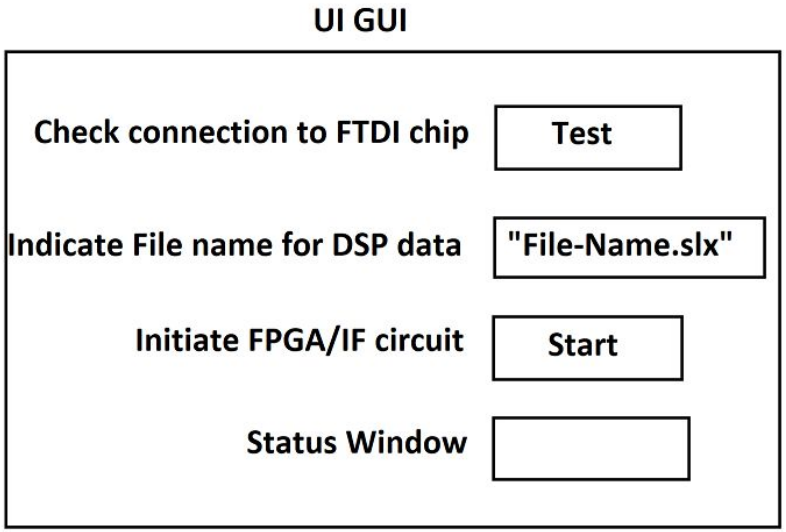
The Intermediate Frequency Circuit **MUST** do the following:

- Digitally generate a periodic signal with a frequency of up to 15 MHz.
- Output Signals through a DAC to the mm-wave radar.
- Return signal from the mm-wave radar (up to 15 MHz) using an ADC.
- The FPGA will send the data to a PC using USB.
- Application on the PC to interface with the FPGA.
- Design PCB for the FPGA interface with the ADC/DAC.

Non-Functional Requirements

Ideally, the Intermediate Frequency circuit **SHOULD** have the following features:

- Have a simple user interface that utilizes a GUI.
- Be written in one of the following languages, C#, Python, Labview, Matlab.
- Require minimal user configuration.
- Compact and portable packaging.
- A PC program that will store the data from the DSP block so that it can be used in Matlab or Labview.
- ADC and DAC with 3.3 V supplies, matching the FPGA.



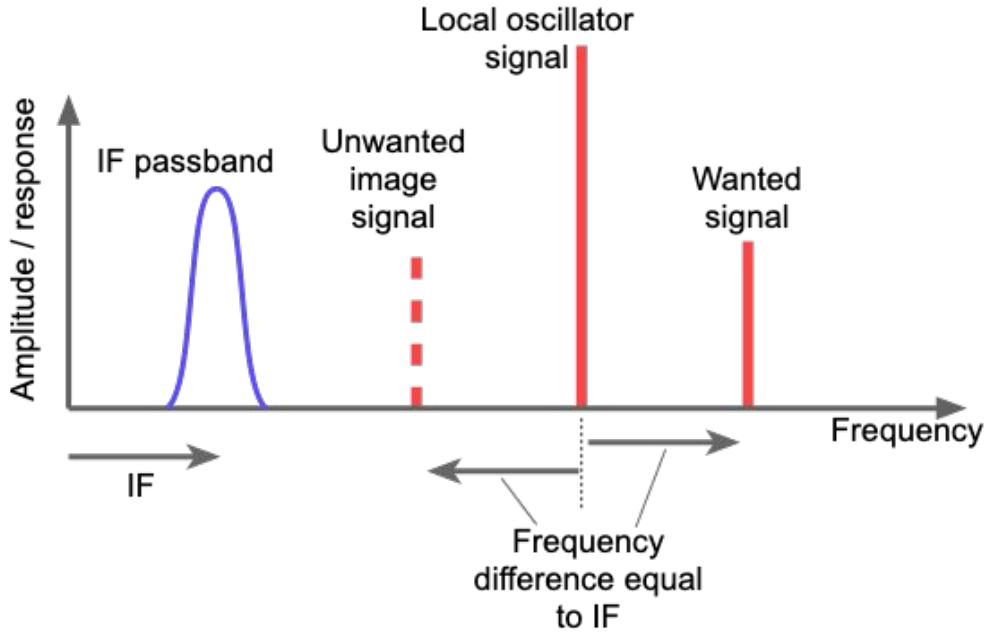
Technical Constraints

Image Rejection

IF circuit must reject signals at the image frequency

Selectivity

IF filter has a specific range (26.5 to 40 GHz) to reject unwanted signals outside of the passband



Technical Constraints

Gain

The IF circuit must provide sufficient gain to amplify the signal to a level that can be further processed by subsequent stages of the receiver

Frequency stability

The IF circuit must be designed to provide stable and accurate frequency conversion to ensure that the signal is demodulated correctly

Potential risks

- Design risks
  - Component selection, circuit layout, and noise.
- Performance risks
  - Quality of the components used, environmental conditions, and interference from other devices.
- Schedule risks
  - Missing deadlines
- Safety risks
  - Minimal, but harsh chemicals and risks of burns with hardware assembly

Mitigations

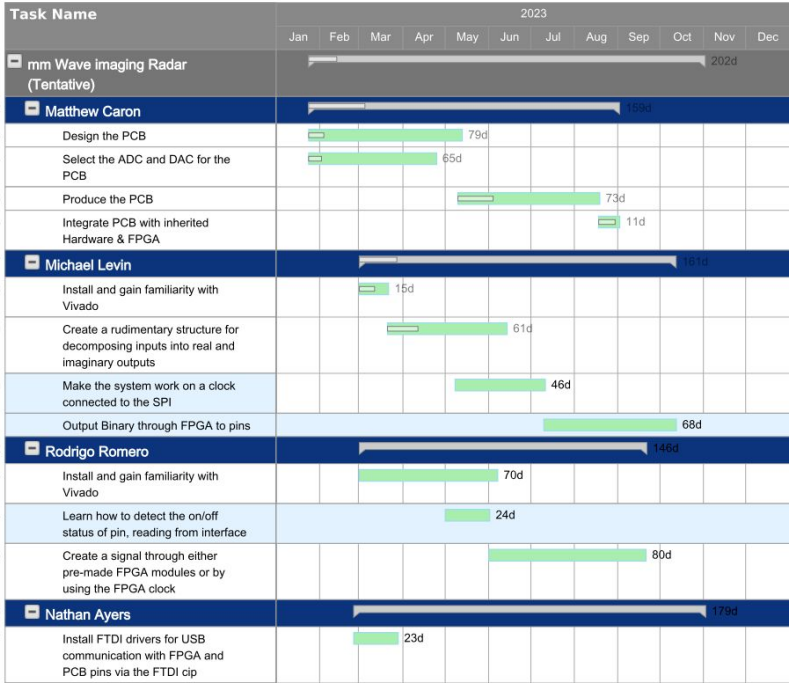
- Design risks
  - Have professionals in the lab to check over work before implementing it.
- Performance risks
  - Simulate designs to determine what tolerances we deem acceptable in the components
- Schedule risks
  - Establishment of accountability between us and our faculty mentor.
- Safety risks
  - Wear PPE when dealing with harsh chemicals

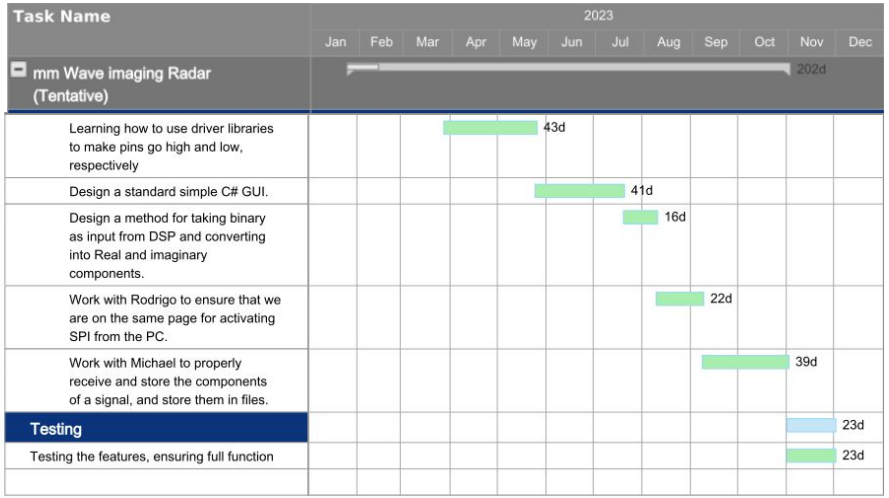
Resource Estimate

Resource	Description	Cost
Labor work	Hours invested in the project by students and faculty mentor	$2500
ADC/DAC	Converters of the circuit	$500
FPGA	Field Programmable Gate Array	$500
Monitor	Displayer of collected information	$300
Accessories	Miscellaneous accessories (USB, cables, 3D printed parts, and others)	$200
TOTAL		$4000

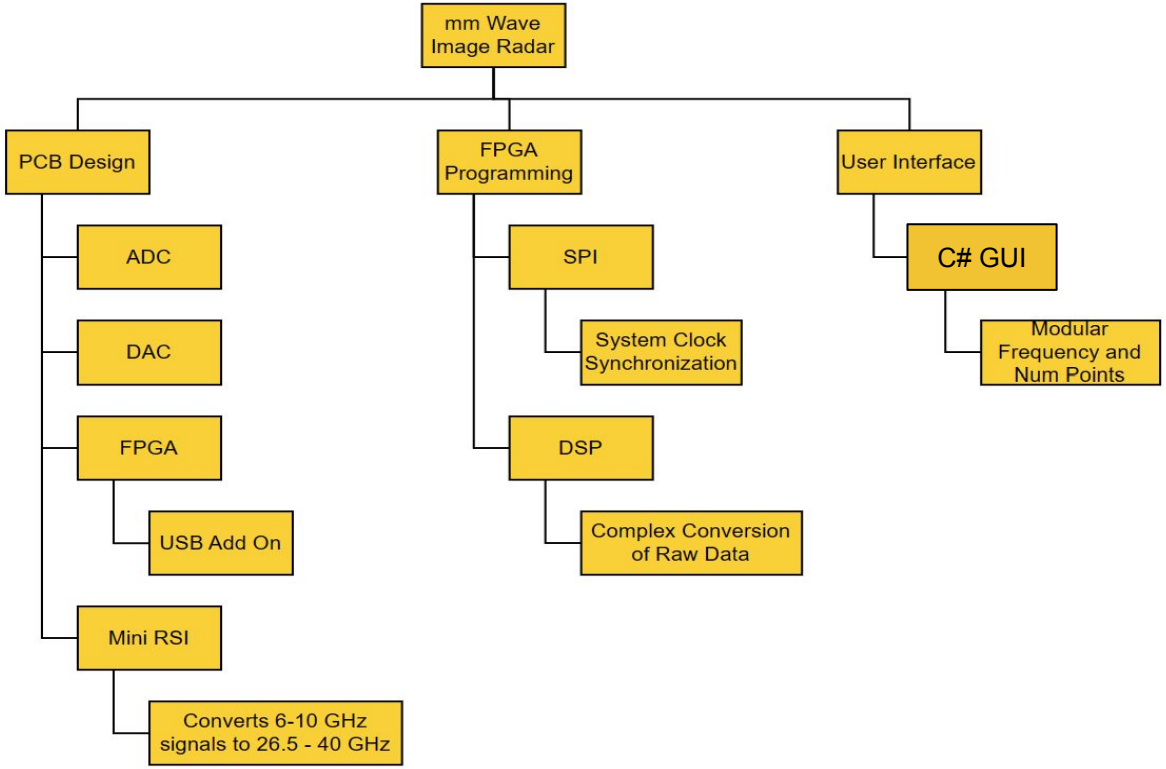
Project Schedule / Milestones

Project Launch Plan

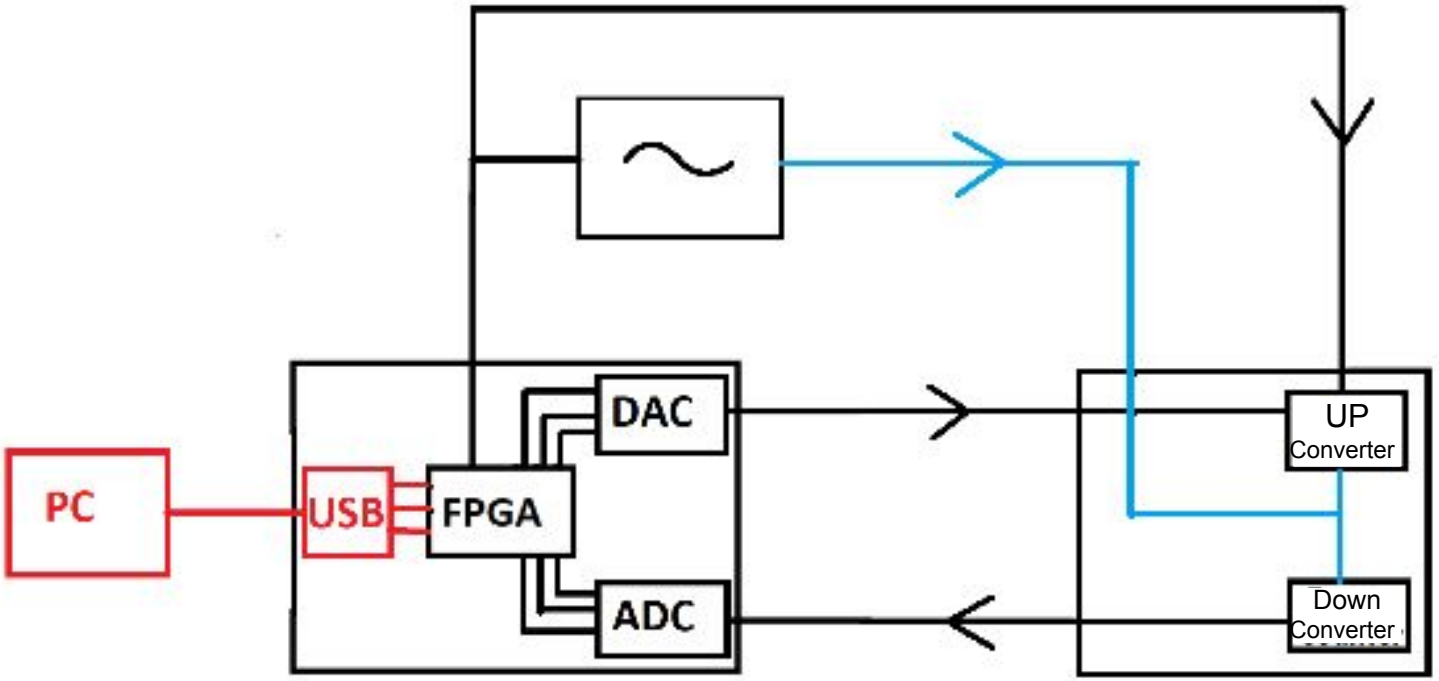




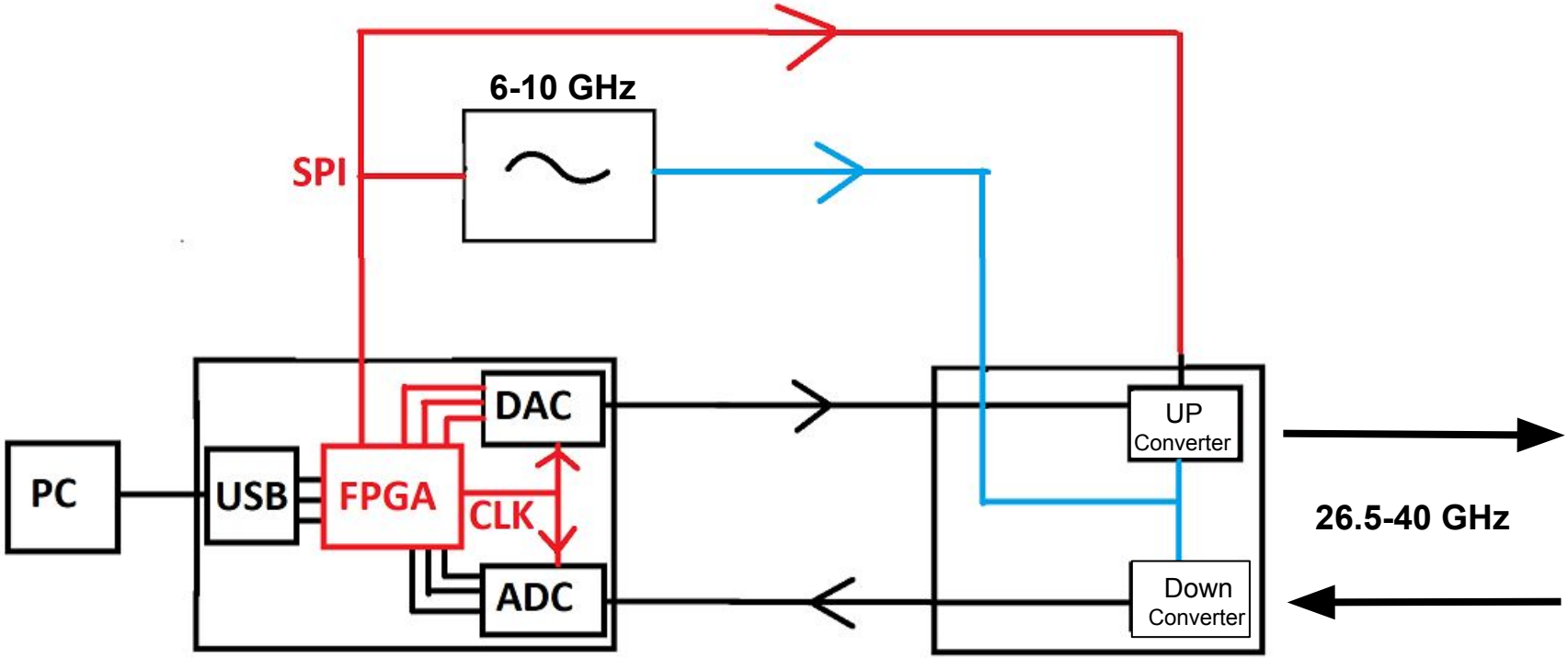
Functional Decomposition



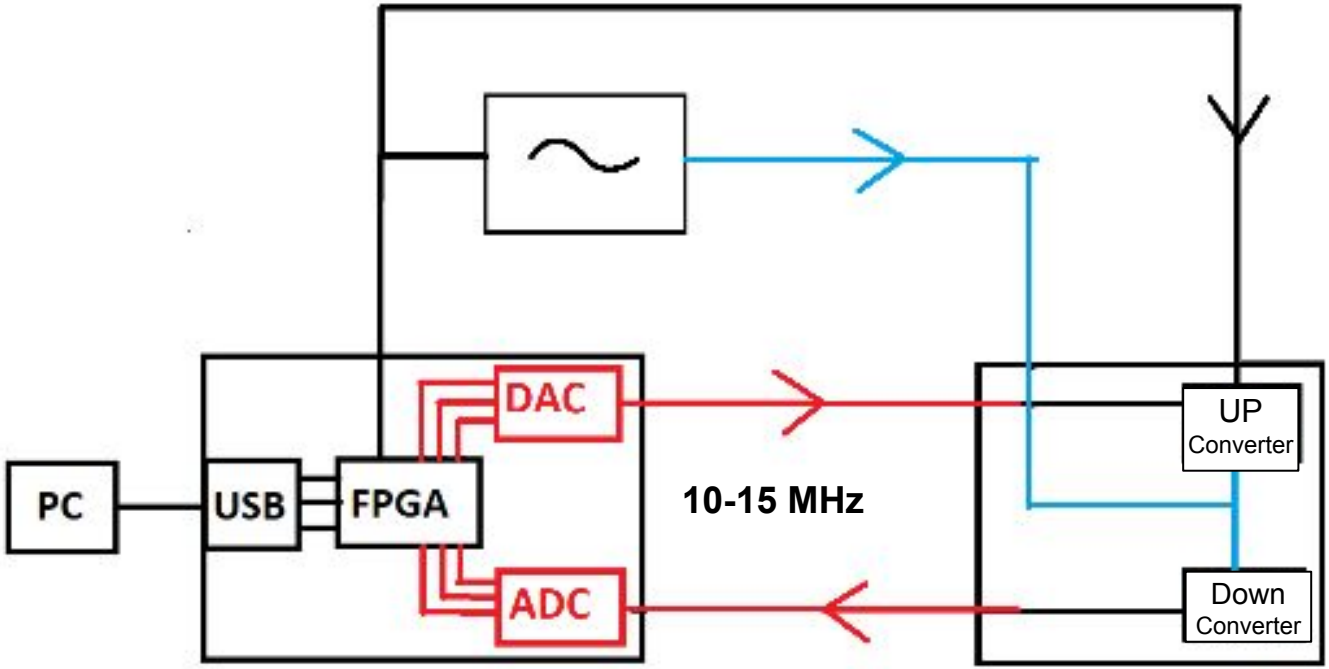
Detailed Design



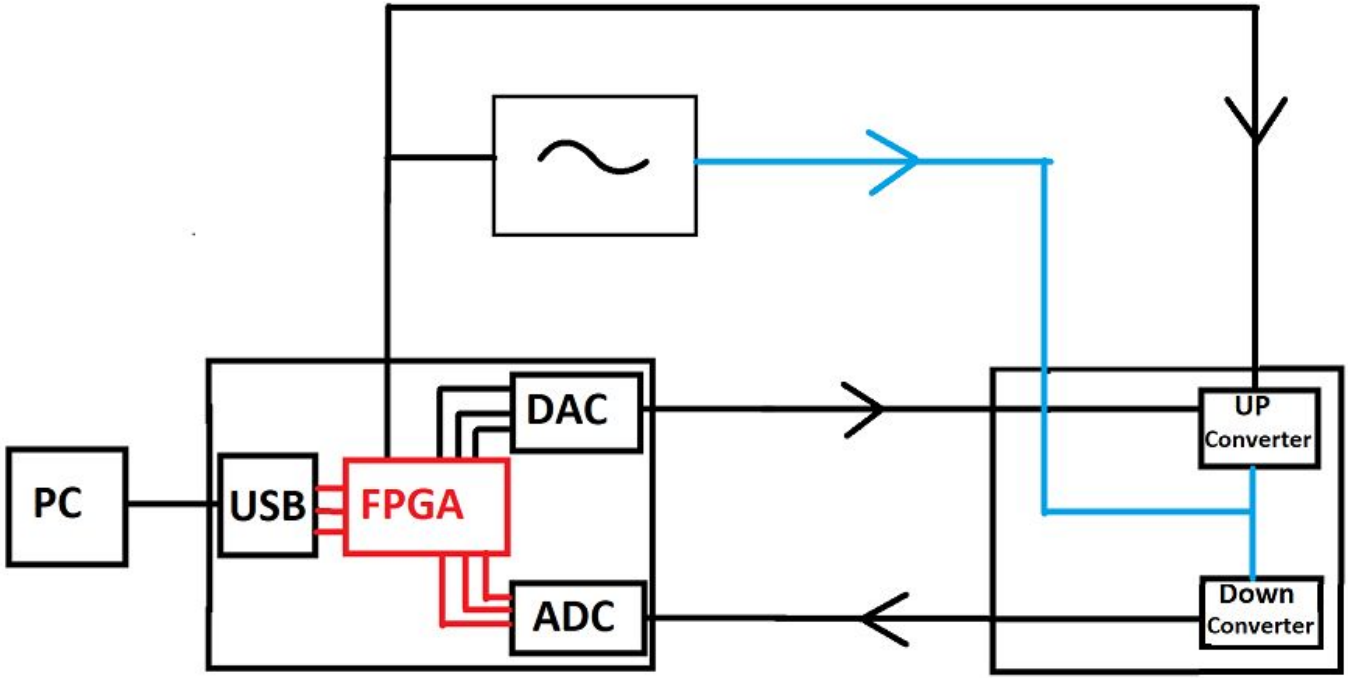
Detailed Design



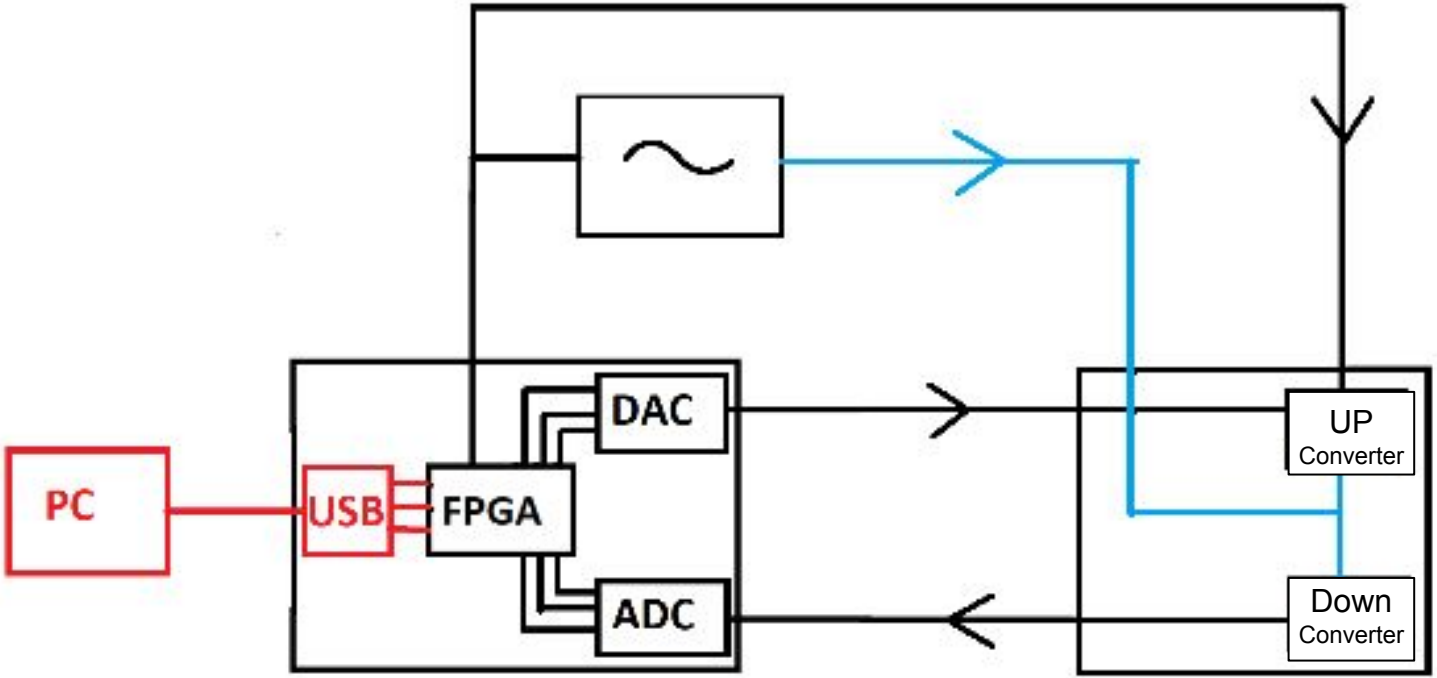
Detailed Design



Detailed Design

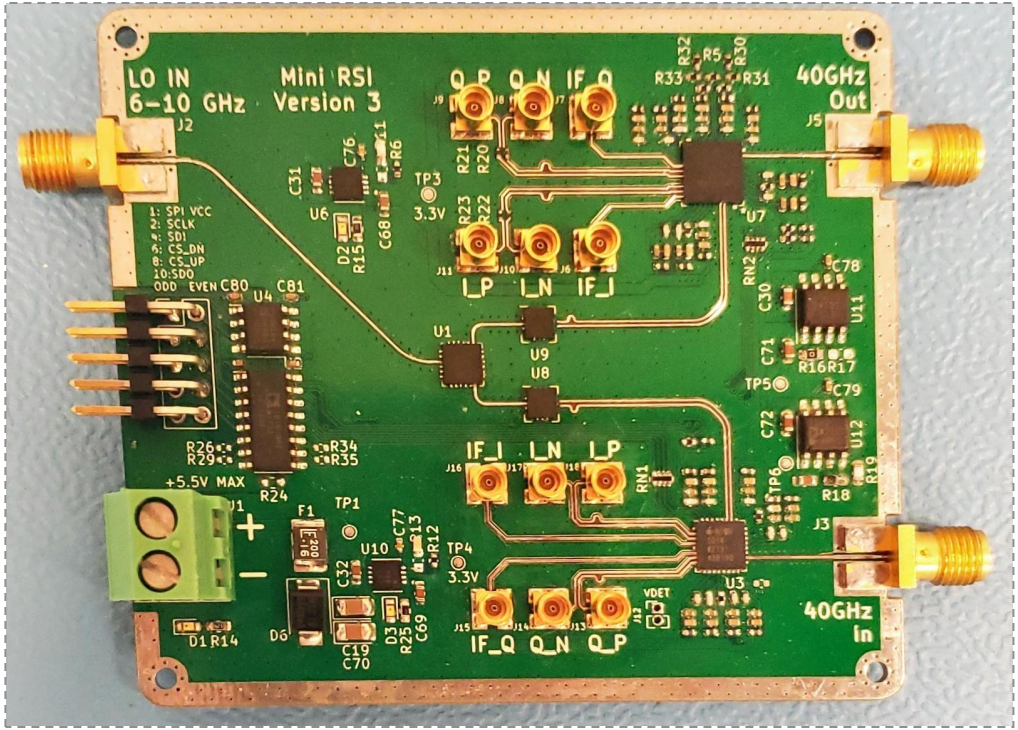


Detailed Design



Chosen Hardware Platforms

- Hardware
  - ADC
    - ADC12DC105
  - DAC
    - AD9767
  - FPGA
    - Xilinx Artix-7
    - FTDI Chip
    - USB - 3.0
  - Mini RSI



Chosen Software Platforms

- SPI
  - Vivado/ Vitis
- DSP
  - Vivado/ Vitis
- FPGA Interface
  - FTDI D3XX Driver
- User Interface
  - C#

```
int main(){
    FT_STATUS ftStatus;
    FT_HANDLE ftHandle;
    FT_DEVICE_LIST_INFO_NODE *devInfo;
    DWORD numDevs;
    // create the device information list
    ftStatus = FT_CreateDeviceInfoList(&numDevs);

    if (ftStatus == FT_OK) {
        printf("Number of devices is %d\n",numDevs);
    }

    if (numDevs > 0) {
        // allocate storage for list based on numDevs
        devInfo = (FT_DEVICE_LIST_INFO_NODE*)malloc(sizeof(FT_DEVICE_LIST_INFO_NODE)*numDevs);
        // get the device information list
        ftStatus = FT_GetDeviceInfoList(devInfo,&numDevs);

        if (ftStatus == FT_OK) {
            for (int i = 0; i < numDevs; i++) {
                printf("Dev %d:\n",i);
                printf(" Flags=0x%x\n",devInfo[i].Flags);
                printf(" Type=0x%x\n",devInfo[i].Type);
                printf(" ID=0x%x\n",devInfo[i].ID);
                //printf(" LocId=0x%x\n",devInfo[i].LocId);
                printf(" SerialNumber=%s\n",devInfo[i].SerialNumber);
                printf(" Description=%s\n",devInfo[i].Description);
                printf(" ftHandle=0x%x\n",devInfo[i].ftHandle);
            }
        }
```

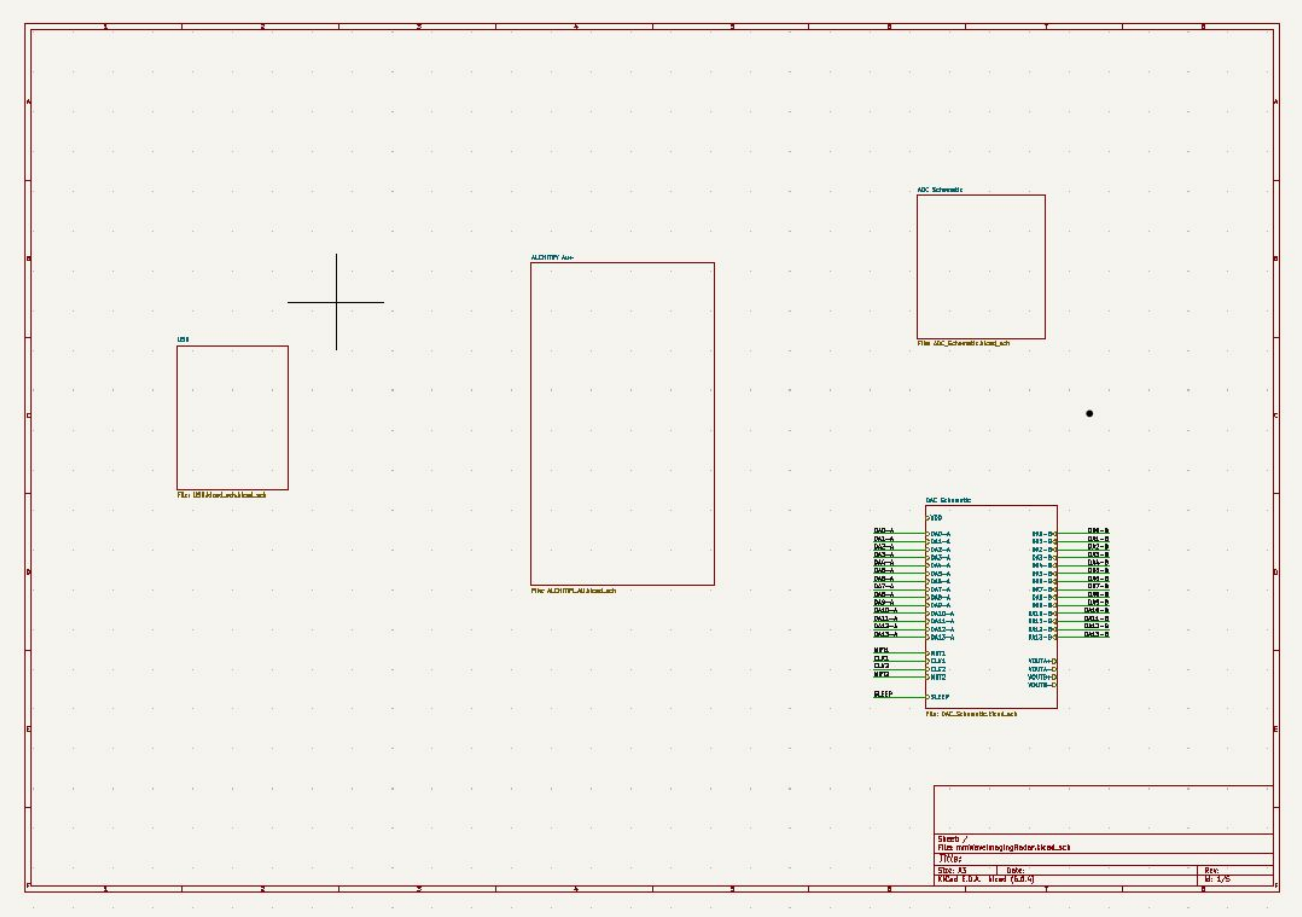
Test Plan

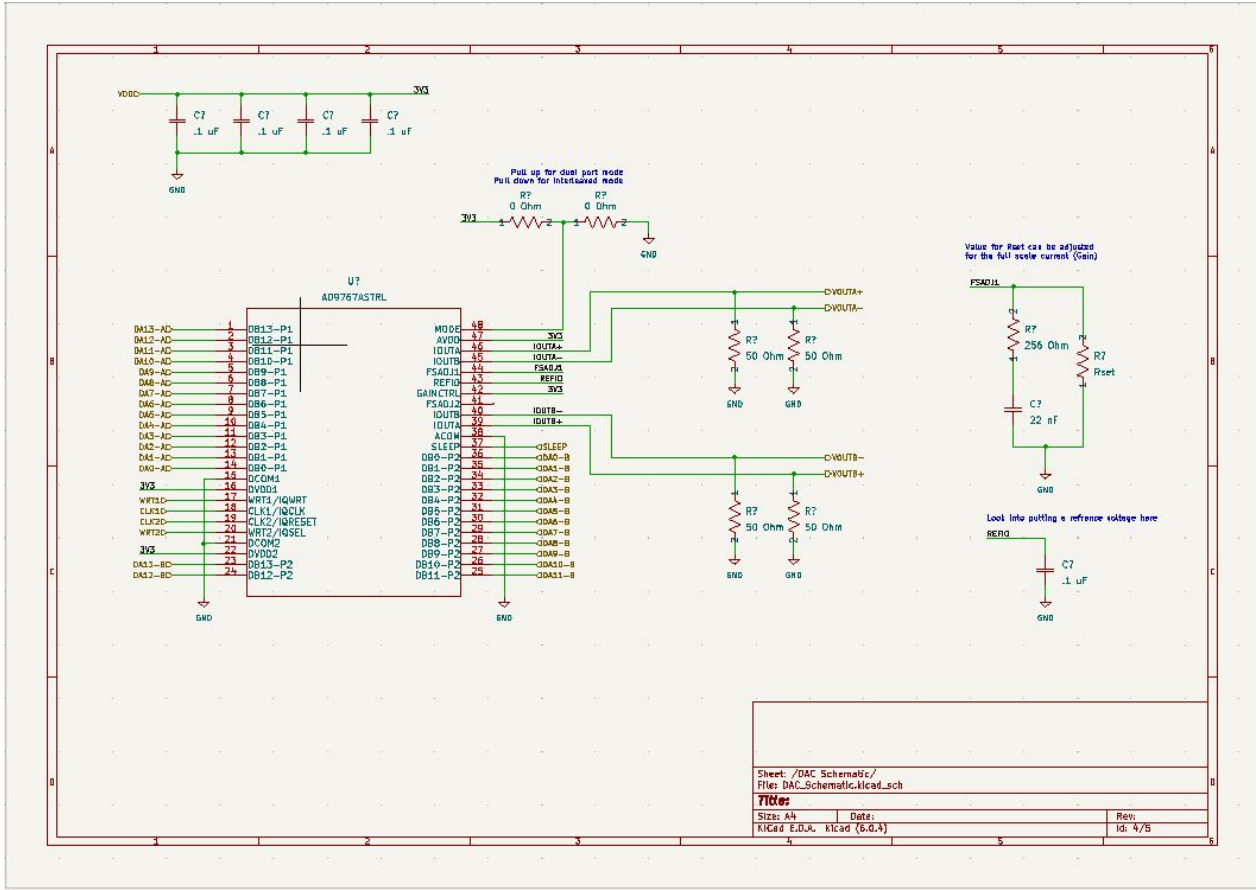
- Hardware
  - Continuity Confirmation
    - Multimeter on all connected components
      - Checking for short/open circuits
  - Signal Confirmation
    - Oscilloscope for all PCB components
      - Confirming cutoff frequencies of ADC and DAC Filters

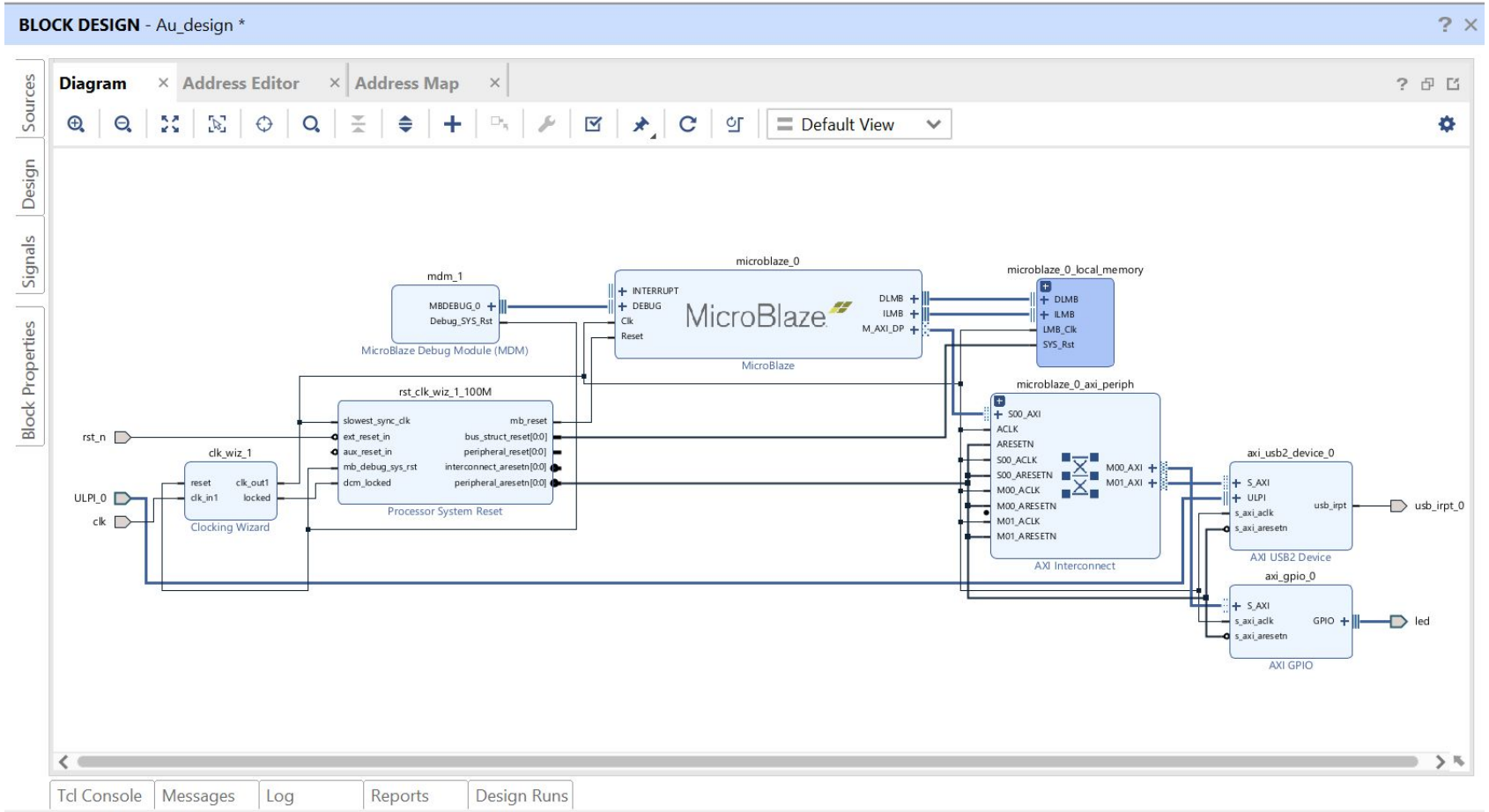
Test Plan

- Software
  - FPGA Interfacing
    - Sending simulated signals to FPGA LEDs
    - Inputting waveforms looking at received data
  - FPGA Program Confirmation
    - Specific waveforms inputs looking at GUI data
    - Input waveforms with GUI looking at SPI output with oscilloscope

Prototype Implementation


ADC Schematic
DAC Schematic


VDDC
3V3
C?
.1 uF
GND
Pull up for dual port mode
Pull down for interleaved mode
R?
0 Ohm
U?
AD9767ASTRL
DB13-P1
DB12-P1
DB11-P1
DB10-P1
DB9-P1
DB8-P1
DB7-P1
DB6-P1
DB5-P1
DB4-P1
DB3-P1
DB2-P1
DB1-P1
DB0-P1
DCOM1
DVDD1
WRT1/IQWRT
CLK1/IQCLK
CLK2/IQRESET
WRT2/IQSEL
DCOM2
DVDD2
DB13-P2
DB12-P2
MODE
AVDD
IOUTA
IOUTB
FSADJ1
REFIO
GAINCTRL
FSADJ2
IOUTB
IOUTA
ACOM
SLEEP
DB0-P2
DB1-P2
DB2-P2
DB3-P2
DB4-P2
DB5-P2
DB6-P2
DB7-P2
DB8-P2
DB9-P2
DB10-P2
DB11-P2
IOUTA+
IOUTA-
IOUTB-
IOUTB+
DAC0-B
DAC1-B
DAC2-B
DAC3-B
DAC4-B
DAC5-B
DAC6-B
DAC7-B
DAC8-B
DAC9-B
DAC10-B
DAC11-B
50 Ohm
VOUTA+
VOUTA-
VOUTB-
VOUTB+
Value for Rset can be adjusted
for the full scale current (Gain)
256 Ohm
Rset
22 nF
Look into putting a refrence voltage here
Sheet: /DAC Schematic/
File: DAC_Schematic.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.0.1)
Id: 4/5

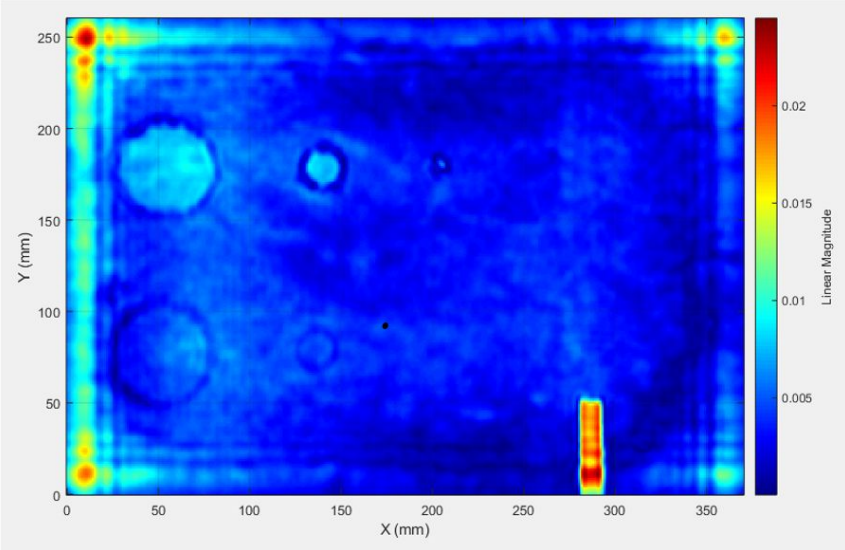

BLOCK DESIGN - Au_design *
Sources
Design
Signals
Block Properties
Diagram
Address Editor
Address Map
Default View
mdm_1
MBDEBUG_0
Debug_SYS_Rst
MicroBlaze Debug Module (MDM)
microblaze_0
INTERRUPT
DEBUG
Clk
Reset
MicroBlaze
DLMB
ILMB
M_AXI_DP
microblaze_0_local_memory
DLMB
ILMB
LMB_Clk
SYS_Rst
rst_clk_wiz_1_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
rst_n
clk_wiz_1
reset
clk_in1
clk_out1
locked
Clocking Wizard
ULPI_0
clk
microblaze_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
axi_usb2_device_0
S_AXI
ULPI
s_axi_aclk
s_axi_aresetn
usb_irpt
AXI USB2 Device
usb_irpt_0
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO
led
Tcl Console
Messages
Log
Reports
Design Runs

Conclusion

- This device will assist researchers at Iowa State to measure a material's dielectric properties at mmWave frequencies
- Some of these properties include:
  - Reflection coefficients
  - Transmission coefficients
  - Dielectric constants

Conclusion

- From these properties we can make many measurements on a material and format the data in a way to image composites to look for flaws (think X-ray but non-ionizing)



Conclusion

This project includes various disciplines of Electrical Engineering

- Hardware
  - FPGA design
  - USB interfacing with the FPGA and PC
  - 2 channel digital to analog conversion
  - 2 channel analog to digital conversion
  - Radar interfacing
- Software
  - Embedded programming (microblaze processor inside the FPGA)
  - USB 3.0 communication between FPGA and PC
  - GUI design for saving and imaging data

Questions?